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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,655	09/25/2003	Yasushi Kinoshita	Q77597	5578

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,655	KINOSHITA, YASUSHI	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/10/01 has been entered. An action on the RCE follows.

2. The amendment filed on 7/08/2005 has been entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tobita, US patent No. 5,801,412.

Regarding claim 1, Tobita teaches (fig. 5) a semiconductor integrated circuit comprising a power supply wiring (VA) and a ground wiring (VB) and a decoupling capacitor (refer to col. 11, lines 40-49) formed between the power supply wiring (VA) and the ground wiring (VB), the decoupling capacitor having electrodes, wherein at least one of the electrodes (electrodes 6c-6f are connected layer 5a and 5a is considered to

be a shield layer) of the decoupling capacitor comprises of a shield layer formed in a plane shape on a semiconductor substrate (1), and the shield layer is connected electrically directly to the semiconductor substrate via a diffusion layer (2d-2i) and is fixed to a power supply potential or the ground potential (refer to fig. 5 and col. 11, lines 40-49) and all of the decoupling capacitor is located outside of a region overlapping with diffusion layer (2d-2i) (if one takes a region where the diffusion region overlaps the region, one can find a decoupling capacitor region that is outside of this region).

Regarding claim 2, Tobita teaches (fig. 5) the entire claimed structure of claim 1 above including another of the electrodes of the decoupling capacitor (9a and 9b), which opposes the electrode comprising the shield layer (5a) includes of a wiring layer (the wiring for either the power supply node or ground line) connected to wirings on an uppermost layer of a multi-layer wiring structure via contact electrodes (the electrodes 9a and 9b also serve as contact electrodes), and a capacitor insulating film (7c and 7c) for forming the decoupling capacitor is provided between the wiring layer and the shield layer (5a).

Regarding claim 3, Tobita teaches (fig. 5) the entire claimed structure of claim 1 above including the shield layer is obtained by covering a plurality of protrusions formed on the substrate (refer to fig. 5).

Regarding claim 4, Tobita teaches (fig. 5) substantially the entire claimed structure of claims 1 and 3 above including a gate electrode (3e-3h).

The limitation that the protrusions are formed simultaneously with the gate electrode by the same formation process for the gate electrode is not given patentable

weight because, this is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 5, Tobita teaches (fig. 5) substantially the entire claimed structure of claims 1 and 3 including the decoupling capacitor is formed on element isolation oxide film (8c-8e).

Regarding claim 6, Tobita teaches (fig. 5) substantially the entire claimed structure of claim 1 above including the shield layer comprises of a silicon compound of a metal (col. 11, lines 23-28).

Regarding claim 7, Tobita teaches (fig. 5) substantially the entire claimed structure of claim 1 above including the decoupling capacitor circuit is formed on an element isolation oxide (8c-8e).

Regarding claim 8, Tobita teaches (fig. 5) substantially the entire claimed structure of claim 1 above including the shield layer comprises a silicon compound of a metal (col. 11, lines 23-28).

Regarding claims 9 and 10, Tobita teaches (fig. 5) substantially the entire claimed structure of claims 1 and 3 above including the diffusion layer (2d-2i) is a well (10) contact diffusion layer.

Regarding claims 11 and 12, Tobita teaches (figs. 5 and 9) the entire claimed structure of claims 1 and 3 above including the semiconductor substrate includes a p-well region and an n-well region. Tobita teaches an example of a CMOS circuit included in the peripheral circuit (Fig. 9A) and CMOS structural inherently implies the formation of both n-well and p-well regions in the semiconductor substrate.

Response to Arguments

5. Applicant's arguments with respect to claims 1-12 have been considered but are not persuasive. Applicant argues Tobita does not disclose, teach or suggest the unique combination of features recited in claims 1 and 3 including the decoupling capacitor of claim 1 and the decoupling circuit of claim 3 which are located outside of a region overlapping with the diffusion layer. The amended claims 1 and 3 recite the limitation of "said decoupling capacitor is located outside of a region overlapping with said diffusion". However applicant does not clearly define what "a region" is. Looking at col. 11, lines 40-49, Tobita clearly teaches that a decoupling capacitor can be implemented by connecting electrode nodes VA and VB to a power supply node and the ground line. It is the connection of nodes VA and VB to a power supply node and the ground line that causes the decoupling capacitor to be formed. As stated above in the rejection, if one takes a region where the diffusion region overlaps the region, one can find a decoupling capacitor region that is outside of this region as in the claimed invention.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
September 18, 2005

Primary Examiner
Steven Loke